RADAR: RET-Aware Detailed Routing Using Fast Lithography Simulations

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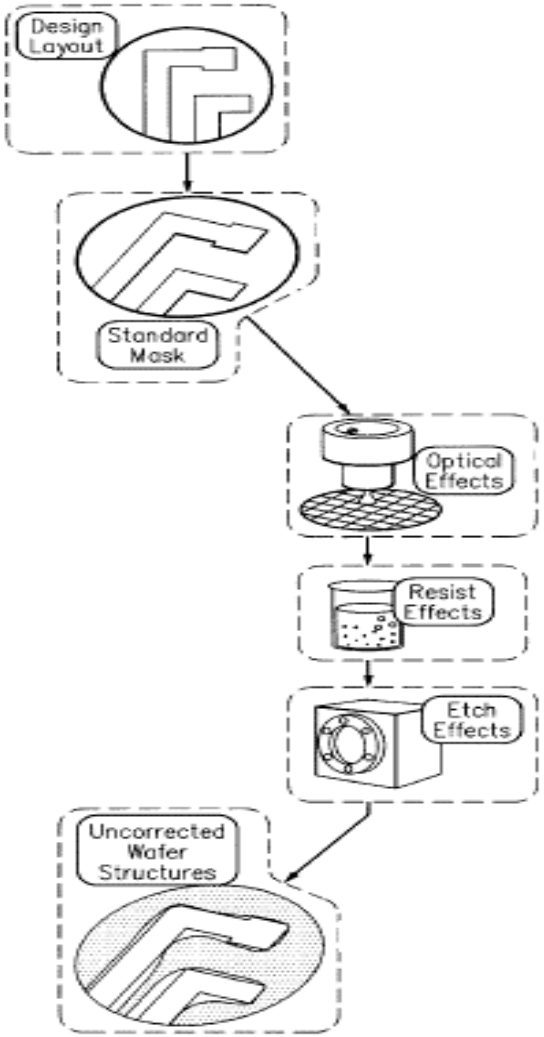
Outline

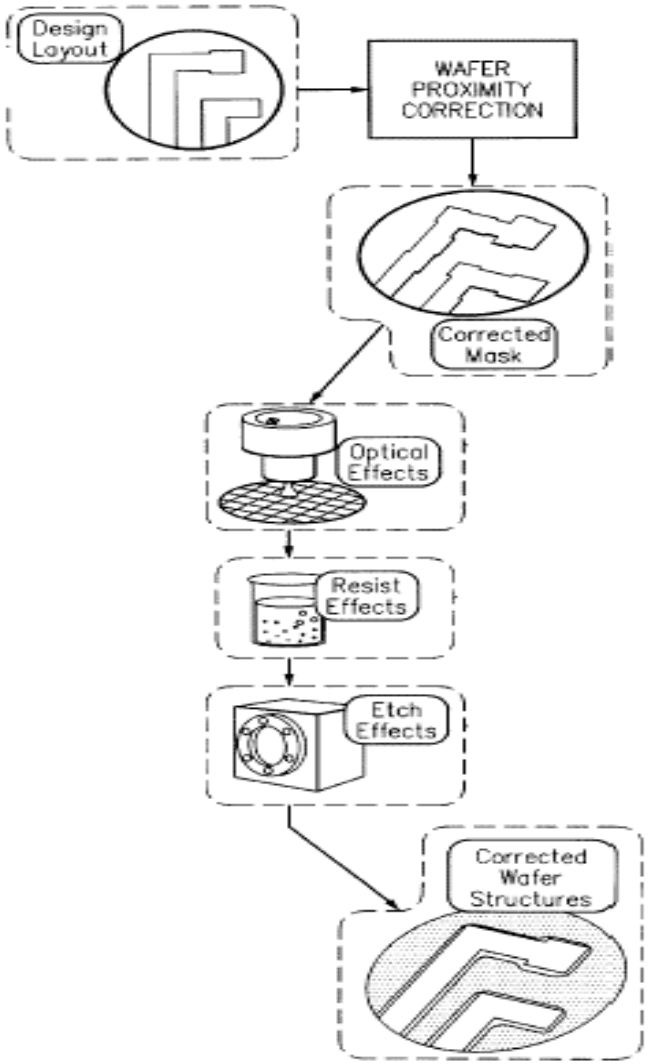
- Lithography Background
- Motivation
- Fast Lithography Simulation
- Edge Placement Error Metric
- EPE map based detailed routing
- Results
- Conclusion

Litho Background

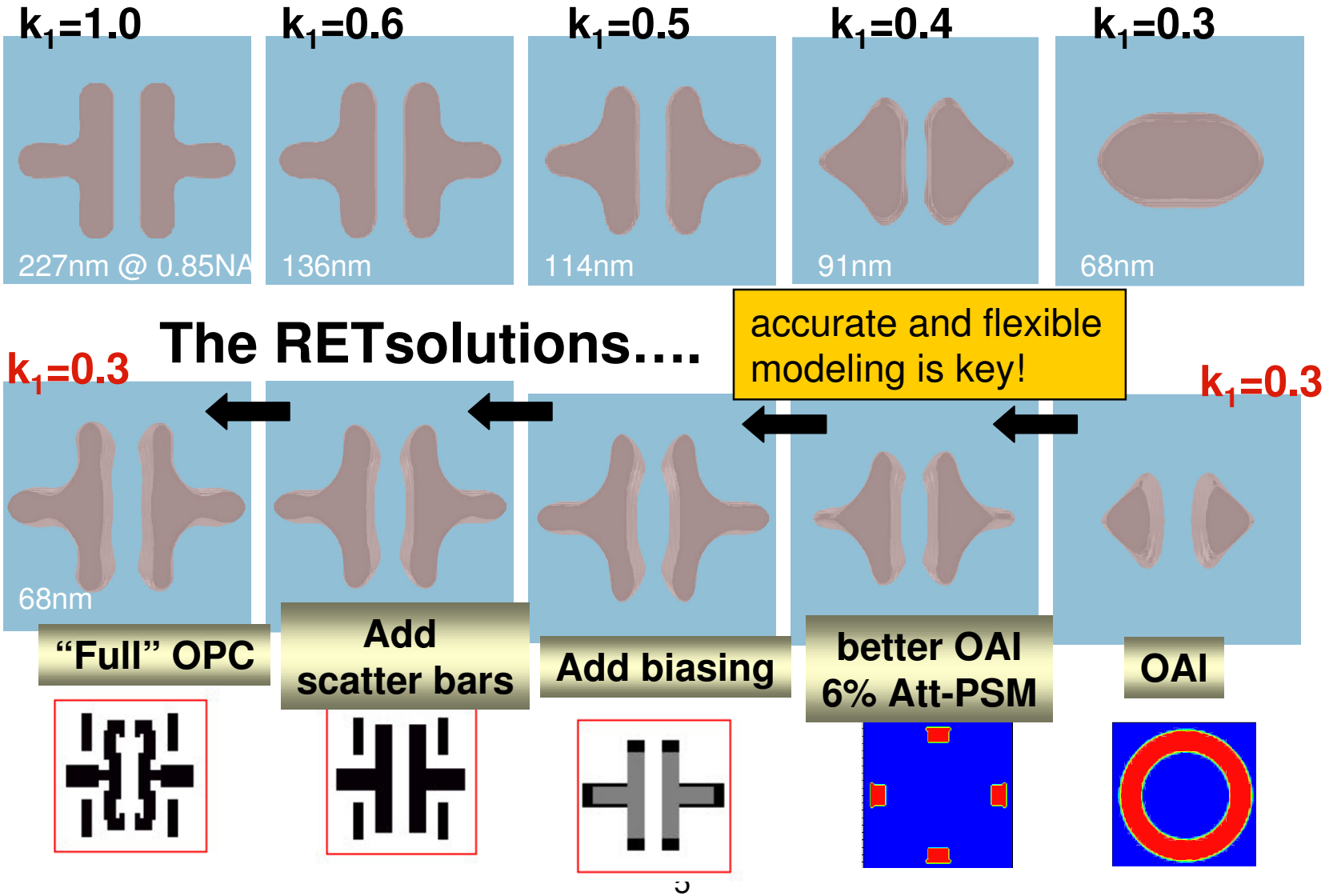
- Lithography limitation is a key bottleneck in nanometer manufacturing
- 193nm wavelength => deep sub-wavelength
- Need extensive RET
  - OPC
  - PSM
  - OAI
- However, RETs mostly are done post-layout
- Major impact from raising the abstraction level RET-aware layout optimization => real DFM

Lithography process with and without OPC





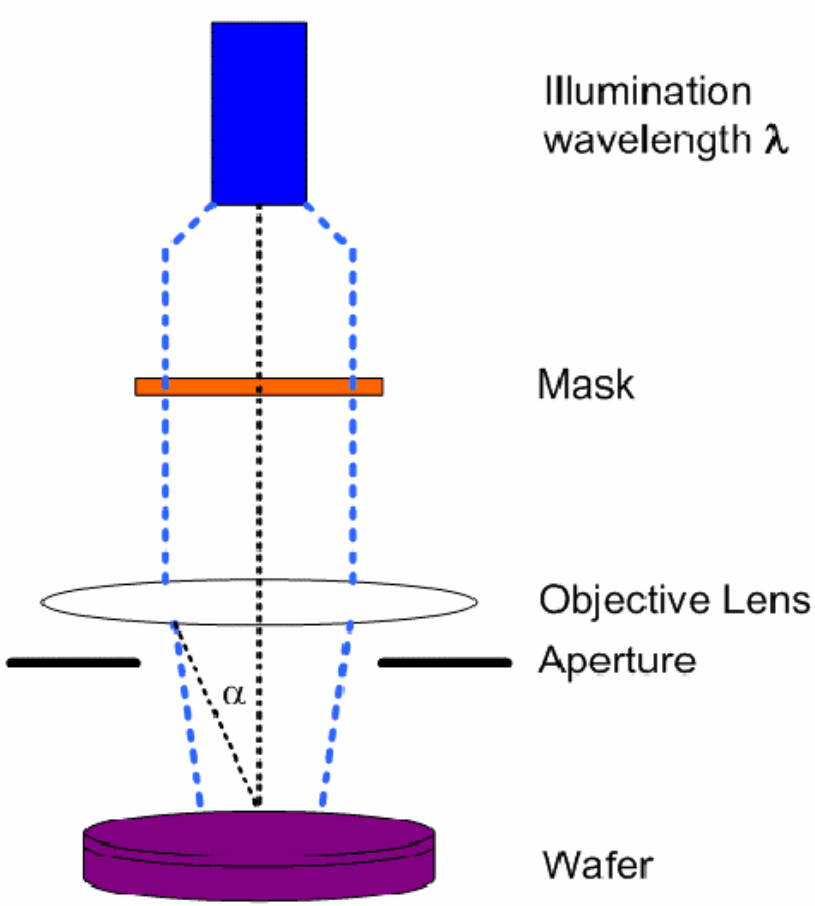
Lithography and RET



(Courtesy ASML)

Fast Aerial Image Simulation

- Fast lithography simulation to generate EPE map
- Aerial image is the first order approximation (resist not considered)
- Basic principle: pre-compute image density convolution table for fast table lookup



Aerial Image Simulation

- For coherent light entering mask:

$$E(x, y) = F^{-1}\{F\{t_m(x, y)\}P(f_x, f_y)\}$$

E = electric field at image point (x, y)

F, F^{-1} = fourier, inverse fourier transforms

t_m = mask transmission function

P = pupil function at objective lens

f_x, f_y = spatial frequencies at image plane

- Intensity equation at image plane

$$I(x, y) = \left|E(x, y)\right|^2 = E \bullet E^*$$

(Cont'd)

- Using principle of superposition and assuming the optics system is a linear space-invariant system, we get the following convolution:

$$E = T_m \otimes h$$

$$T_m = \text{mask transmission function}$$

$$h = \text{impulse response function}$$

$$I = E \bullet E^*$$

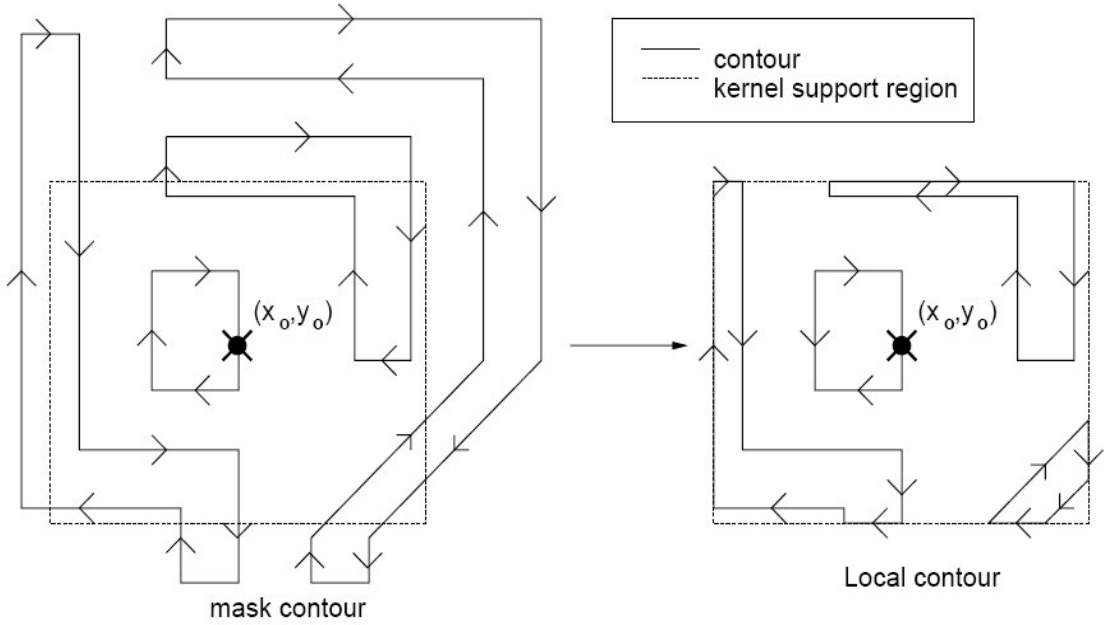
(Cont'd)

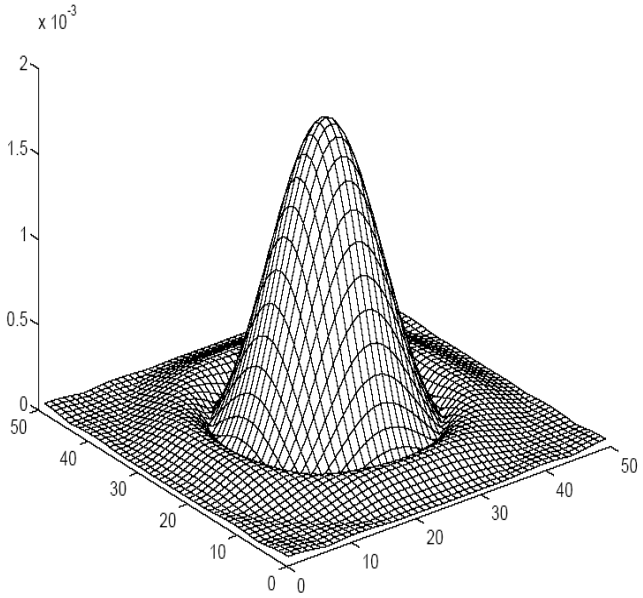
- In reality, for accurate simulation, the following corrections are needed:
  - Partially coherent light. Extend to Hopkin's model.
  - Incorporate effect of lens aberrations into pupil function P.
  - Effect of defocus. Add phase error to higher diffraction orders.

Fast aerial image simulation

- Modern techniques by
  - [Cobb]
  - [Stirniman et. al]
  - [Pati et. Al]
- Basic principle: Precompute convolutions and store for fast table lookup.
- Our approach is a variation of [Cobb].
- Precompute all possible upper rectangular convolutions within a support region.

(Cont'd)





- Support region = 1-4μm in perimeter or a multiple of resolution=?/NA

Edge Placement Error Map

- A concept similar to congestion or thermal hotspot
- Measurement of RET effort
- Work seamlessly with existing CAD flow

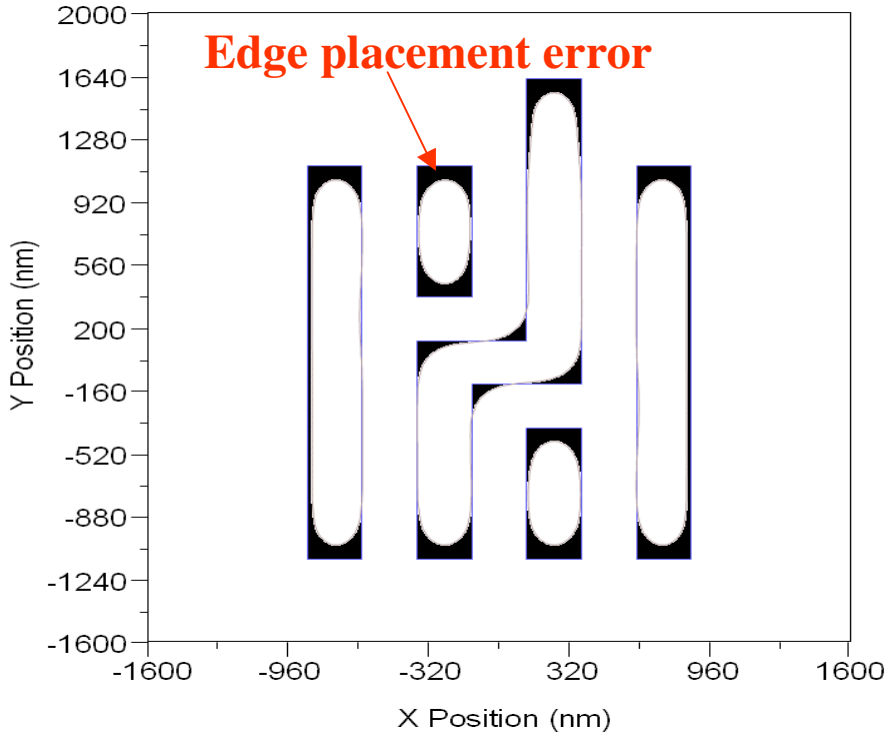
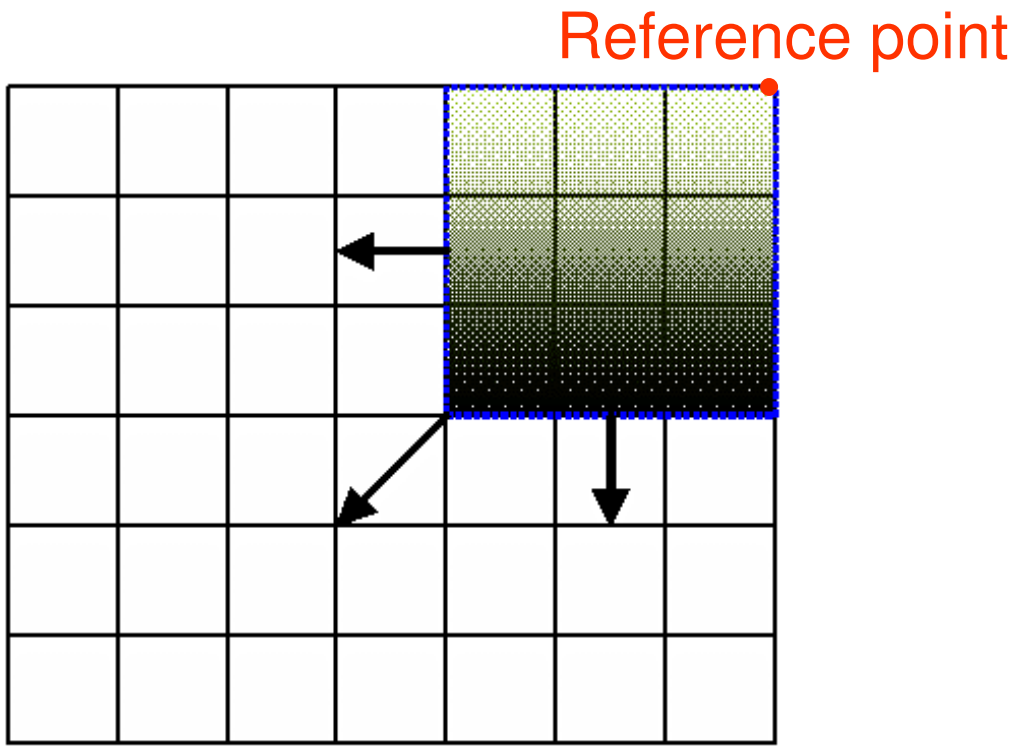
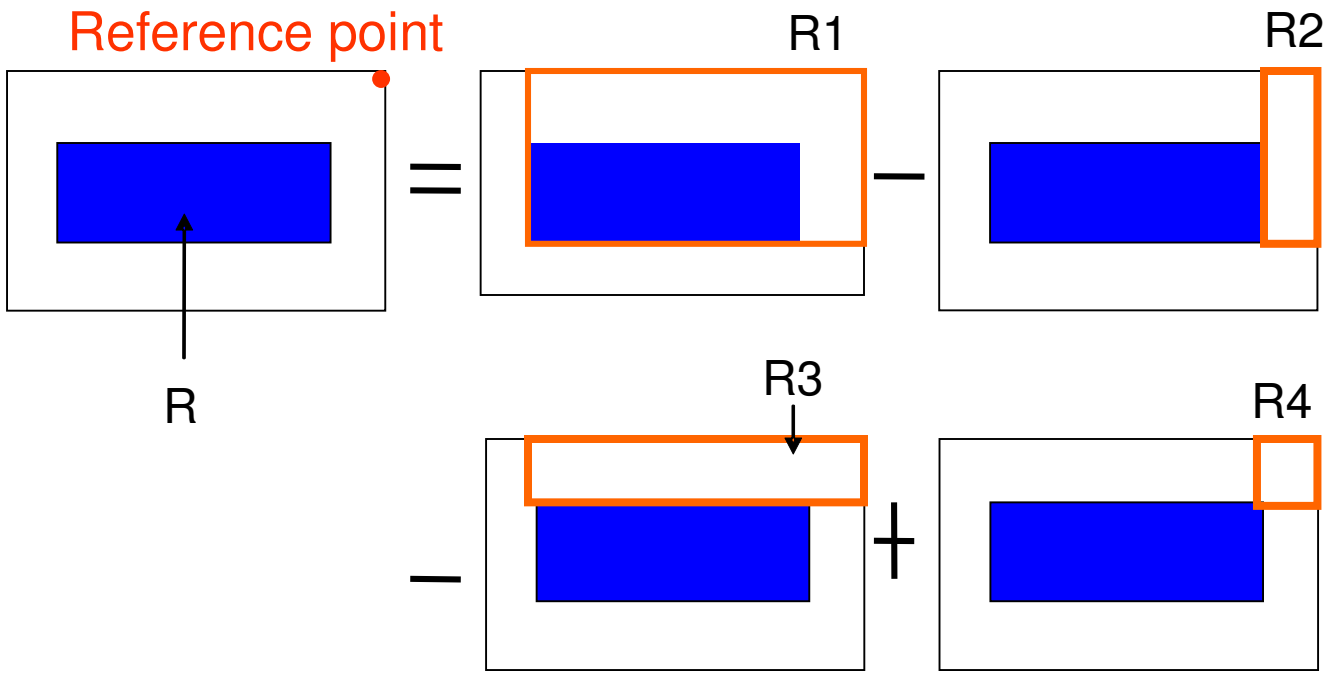


Table Look-up



- Store convolution table for rectangles w.r.t the top-right reference point

Table Look-up Example



$$conv(R) = conv(R1) - conv(R2) - conv(R3) + conv(R4)$$

EPE Map

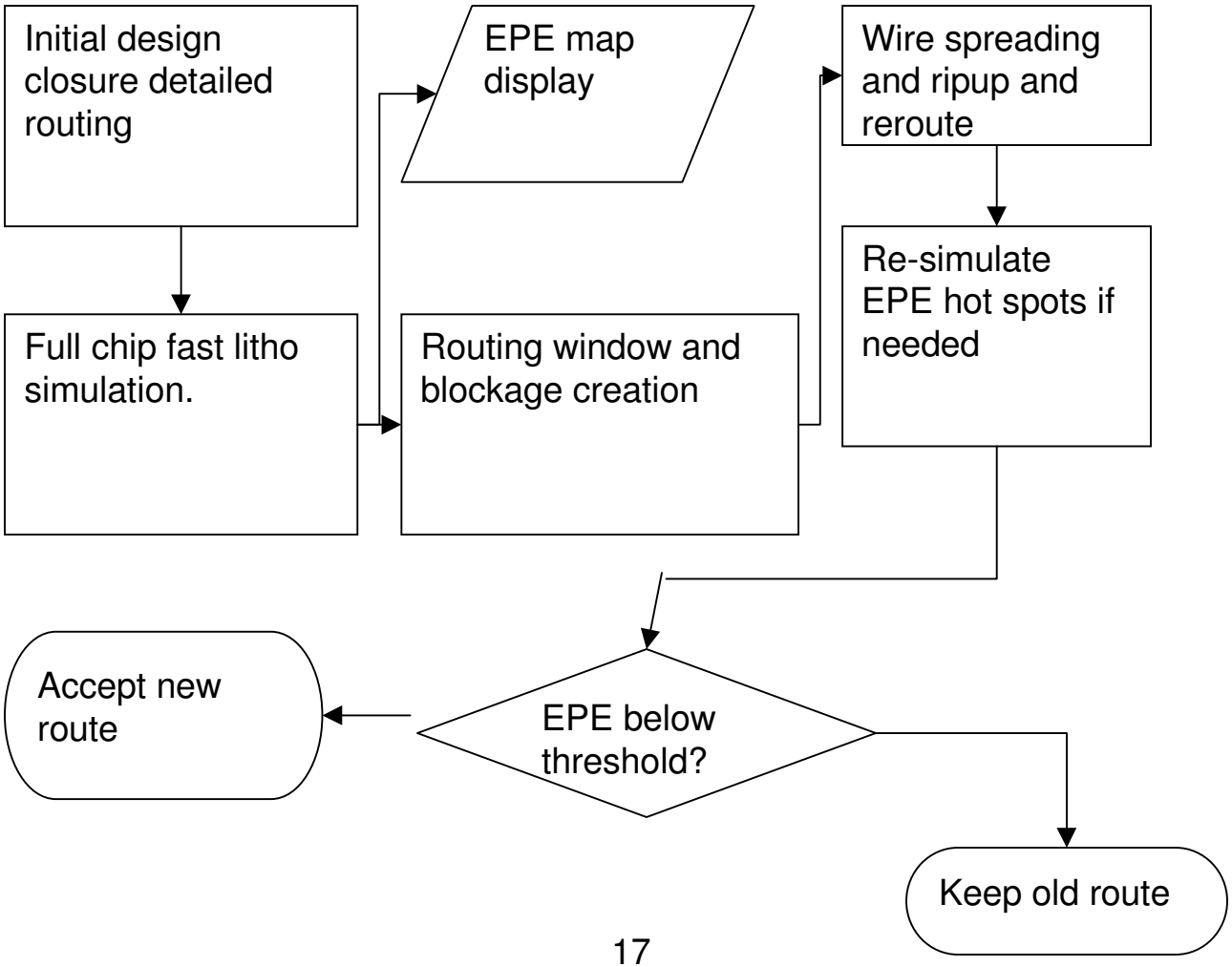
- Generate EPE for each “control point” (points that may have large edge placement errors) in design
- Each EPE control point has a ranked list of neighboring wires that contribute to the EPE
- Abstract a normalized EPE density for an entire routing segment

$$EPE_{avg} = \frac{\sum_{i=1}^{N} EPE_i}{N}$$

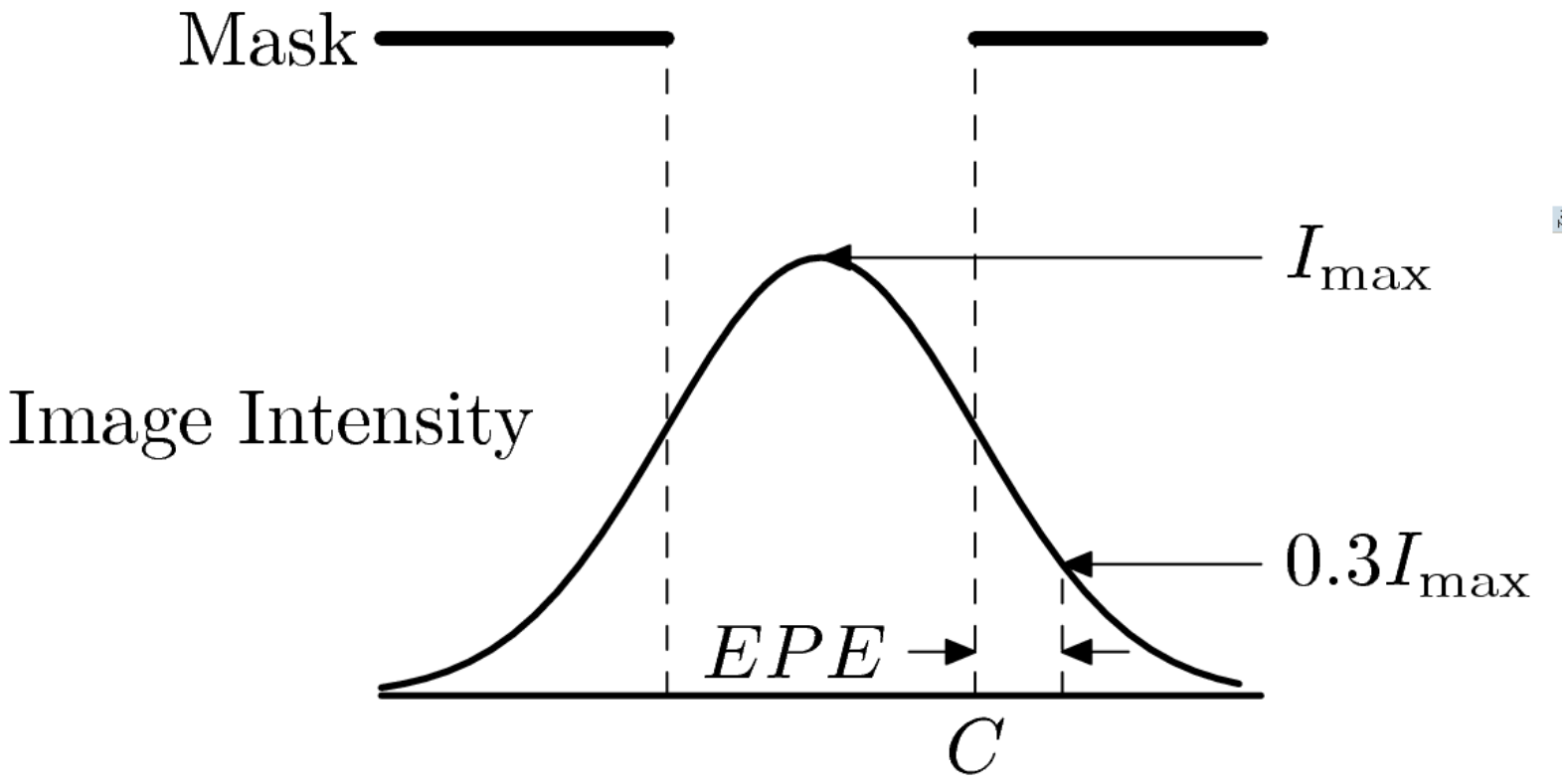
RADAR: RET-Aware Detailed Routing

- Use EPE map to guide RADAR
  - Do not need to run lithography simulations often
- Rip-up-and-reroute
  - Focus on EPE hotspots
  - Re-simulate EPE only if necessary (rerouted regions)
  - Store EPE influencing neighbor list for router to avoid those neighbors with high EPE impacts
- Routing blockage generation and wire spreading
  - Protect safe regions with low EPE

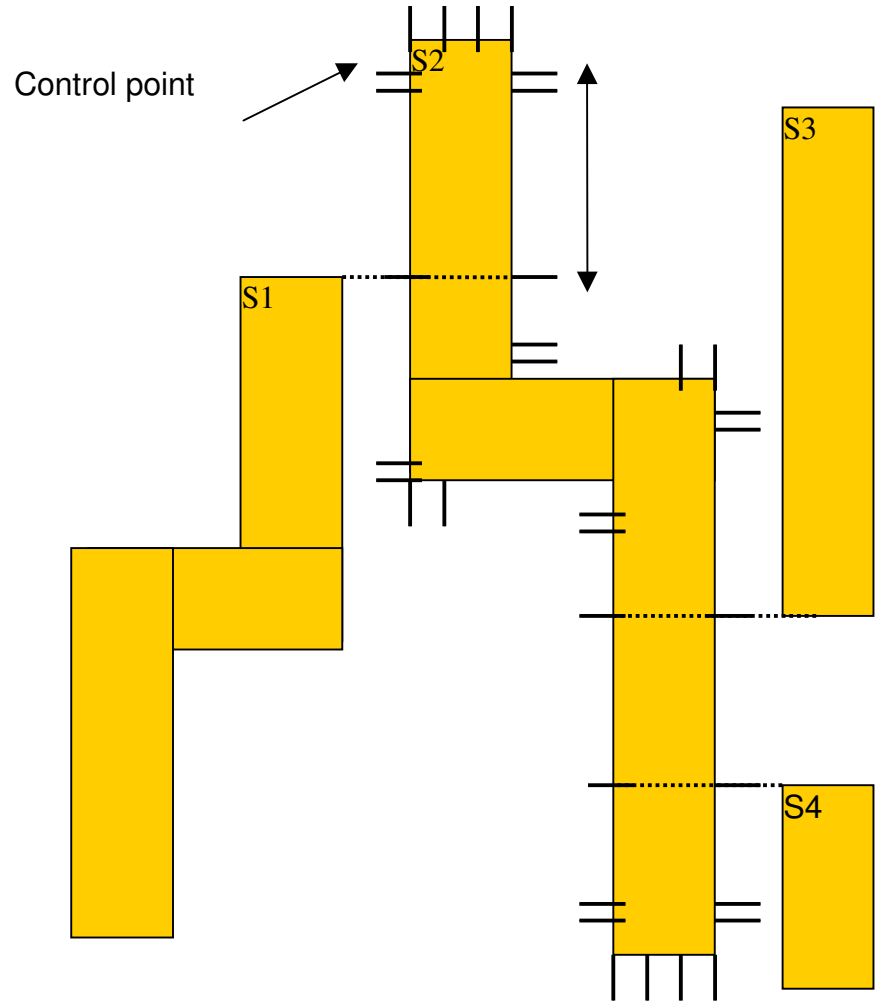
EPE correction flow



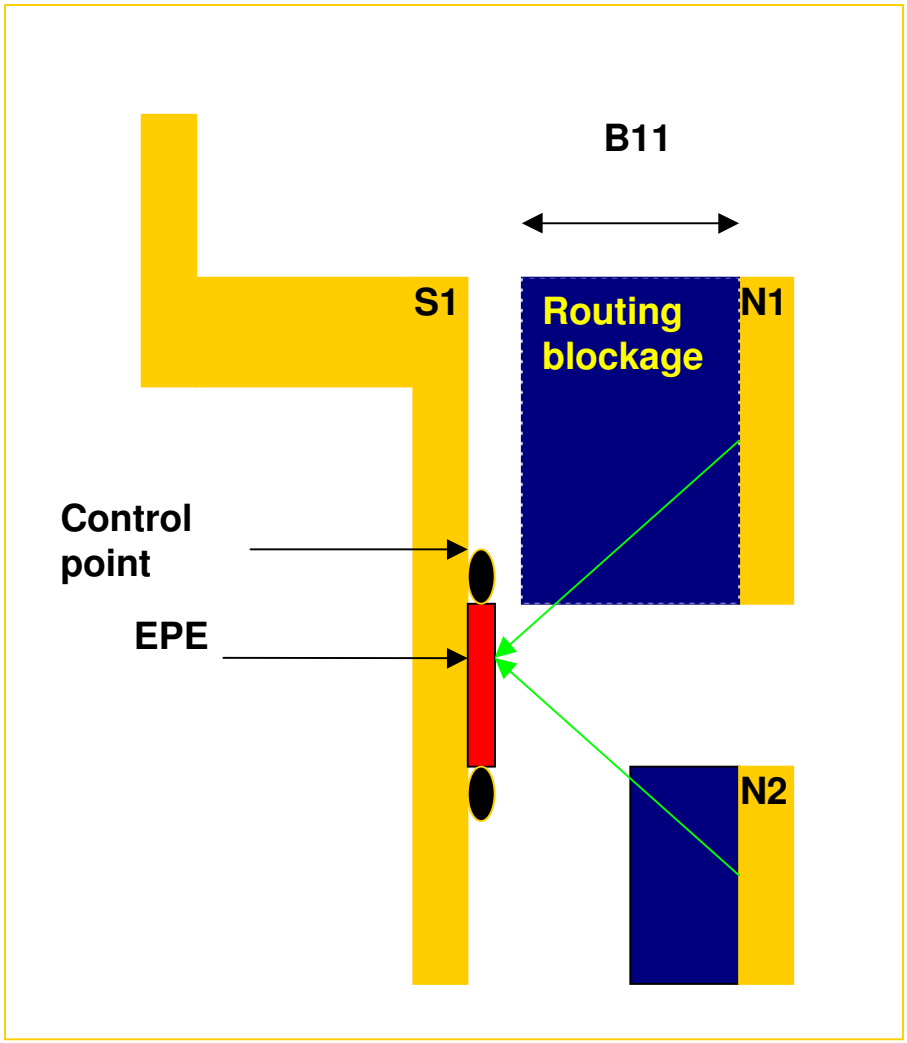
EPE cutline computation

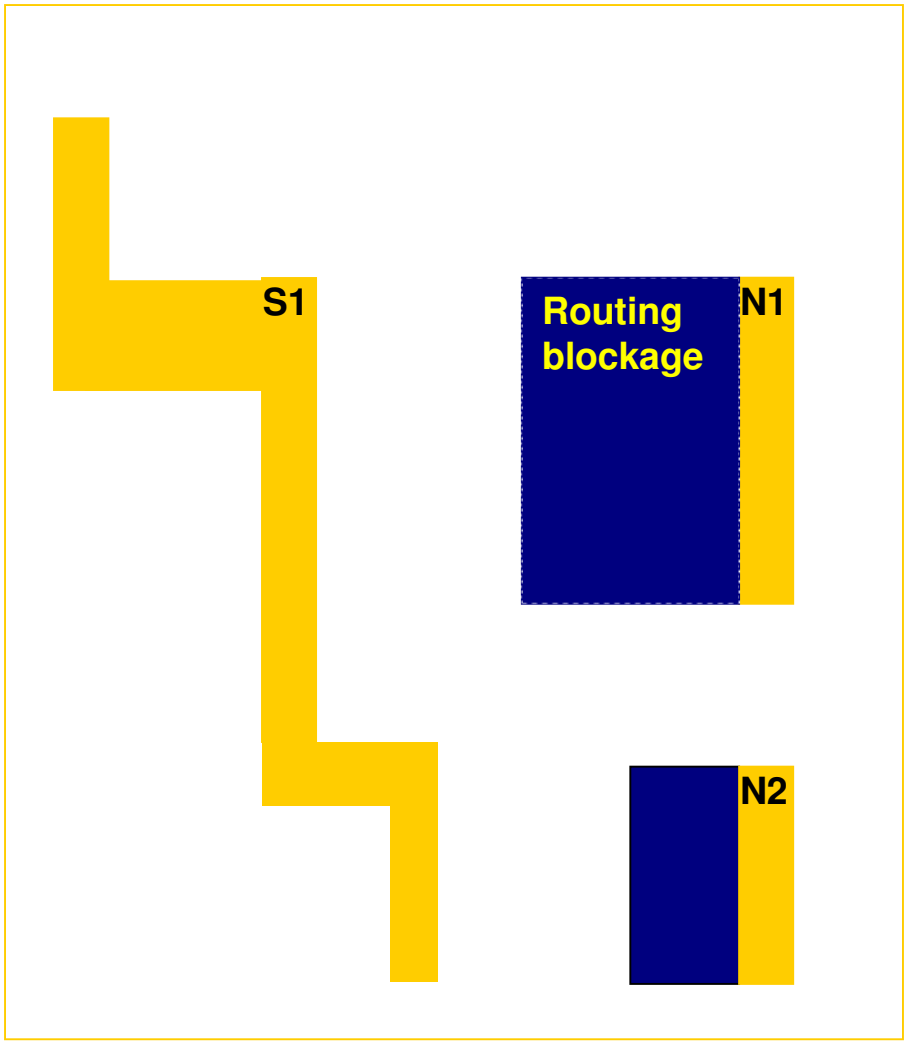


Control point generation

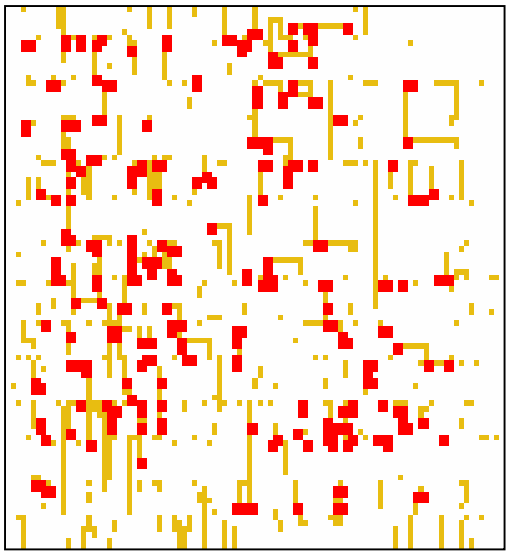


Intelligent Ripup & Reroute

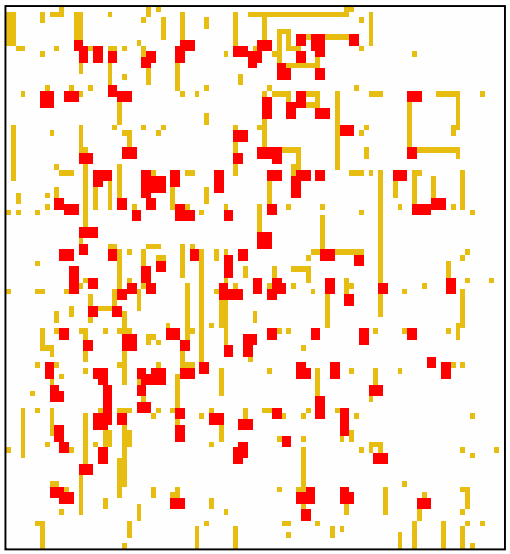




Experimental Results on a 65nm Industry Design

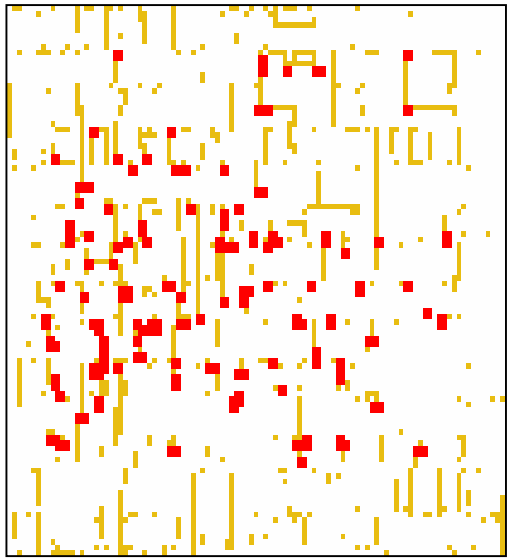


Initial routing (after design closure)



After wire spreading:

12% EPE reduction with 10% WL increase



After R&R:

40% EPE reduction
5% WL increase

Experimental Results

Design	Original EPE	Spread EPE	R&R EPE	Spread WL	R&R WL
Ckt1	81	71	54	5%	2%
ckt2	720	612	468	20%	5%
ckt3	541	486	362	11%	5%

- EPE reduced by 40%
  - wirelength increased 5%

Conclusions

- Raised Lithography modeling up to design implementation level.
- EPE map manufacturing effort metric.
- Two routing techniques to reduce EPE.
- RR using blockages showed promising results.
- Future research directions:
  - Further model speedup to enable correct-by-construction litho-friendly routing.
  - New manufacturing-friendly detailed routing algorithms.