

CALL FOR PARTICIPATION – EDP 2002



Design Automation
Technical Committee
DATC

ELECTRONIC DESIGN PROCESSES 2002
APRIL 21-23, 2002

MONTEREY BEACH HOTEL,
MONTEREY, CALIFORNIA
<http://www.eda.org/edps/edp02>



The Electronic Design Processes (EDP) Workshop provides a forum for a cross-section of the design community to discuss state-of-the-art electronic design processes and CAD methodologies. As the requirements and complexities of electronic design increase, past ad hoc approaches to design processes are proving inadequate. The workshop focuses on the improvement of the overall design process, rather than on the functions of the individual tools themselves. The core audience of EDP consists of CAD system integrators and methodologists, academic researchers, and design team managers.

STILL ^

Focus in 2002: It's ^ the Methodology, Stupid!

ADVANCE TECHNICAL PROGRAM

Monday, April 22

KEYNOTE 1 "Decreasing Product Development Cycles in a Rapidly Growing Company", Dan Smith (Nvidia)

SESSION 1: HIGH-LEVEL MODELING I

1.1 "The Future of High-Level Modelling and System Level Design: Some Possible Methodology Scenarios", Grant Martin (Cadence Design Systems)

1.2 "Bridging the High-level and Implementation Divide: Mission Impossible?", Victor Konrad (Intel)

1.3 "SystemC abstractions and design refinement for HW-SW SoC designs", Dunder Dumlugol (CoWare/SystemC)

1.4 "SpecC Methodology for High Level Modeling", Rainer Doemer (UCI/SpecC)

1.5 "High-level Design Using General-Purpose Languages", John Sanguinetti (FORTE/Cynlib)

Panel : High Level Modeling Methodology: Will it ever be mainstream?

SESSION 2: HIGH-LEVEL MODELING II

2.1 "A Methodology for SoC Top-Level Validation using Esterel Studio", Lionel Blanc, Amar Bouali, Jérôme Dormoy and Olivier Meunier, (Esterel Technologies)

2.2 "Breaking Down Complexity for Reliable System-Level Timing Validation", Dirk Ziegenbein, Marek Jersak, Kai Richter and Rolf Ernst, (Technical University of Braunschweig)

2.3 "TACO: Rapid Design Space Exploration for Protocol Processors", Seppo Virtanen, Johan Lilius, Tero Nurmi and Tomi Westerlund, (Turku Centre for Computer Science)

SESSION 3: HW/SW CO-DESIGN

3.1 "Platform-based Design: Report from the Front", Daniel Martin, Sagheer Ahmad, and Kambiz Khalilian (Infineon Technology)

3.2 "Platform-Based Design and the First Generation Dilemma", Jiang Xu and Wayne Wolf (Princeton University)

3.3 "Platform-based Co-Design and Co-Development: Experience, Methodology and Trends", Grant Martin and Jean-Yves Brunel (Cadence Design Systems)

Invited Talk "Evolving ASIC Methodology to Adapt to Technology and EDA Tool Advances", Tom Russell (IBM)

Tuesday, April 23

SESSION 4: RTL METHODOLOGY

4.1 "Managing Risk in Block Based Designs: A Front End Acceptance Methodology", Kumar Venkatramani and Stefanus Mantik (Cadence Design Systems)

4.2 "Policy-Based RTL Design", Bhanu Kapoor and Bernard Murphy (Atrenta)

SESSION 5: THE FUTURE OF RTL SIGNOFF

5.1 "Design Tool Advances Drive ASIC Signoff Paradigm Shift", Tom Russell (IBM)

5.2 "Providing Physical Vision to RTL Designers", Shankar Krishnamoorthy (Synopsys)

5.3 "TANSTAF: There ain't no Such Thing as a Free Lunch", Paul Rodman (Reshape)

5.4 "Noise in the RTL Signoff Flow", Vivek Joshi (Intel)

5.5 "Evolution of Sign-off Models", Tommy Eng (Tera Systems)

5.6 "TBD", Dan Deisz (LSI Logic)

KEYNOTE 2 "Collaboration Methodologies and Best Practices for IP Development and SOC Design", Dennis Harmon (Synchronicity)

SESSION 6: ANALOG MIXED SIGNAL

6.1 "A New Methodology for Analog/Mixed-Signal (AMS) SoC Design that Enables AMS Design Reuse and Achieves Full-Custom Performance", Kazuhiro ODA (Toshiba), Lou Prado, and Anthony J. Gadiant (NeoLinear)

6.2 "Synthesizable full custom mixed signal IP", Mar Hershenson and Dave Colleran (Barcelona Design)

6.3 "A Revolutionary New Solution to Unified RF Systems and Circuit Design", James Spoto (Applied Wave Research)

SESSION 7: COST-EFFECTIVE DESIGN

7.1 "Cost Savings through Reuse", Aparna Dey (Synchronicity)

7.2 "IP Authoring and Integration for HW/SW Co-Design and Reuse - Lessons Learned", Frank Schirrmeyer, Martin Meindl and Stan Krolikoski (Cadence Design Systems)

7.3 "Reuse and Quality Enhancement via Computation and Distribution of Component Derivative Rewards", Juan-Antonio Carballo, W. Belluomini and R. Montoye (IBM Research)

WORKSHOP ORGANIZATION

Steering Committee

David Hathaway (IBM)

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