



Physical Design Methodology Best Practices

NANOMETER AND RTL-DOWN CLOSURE

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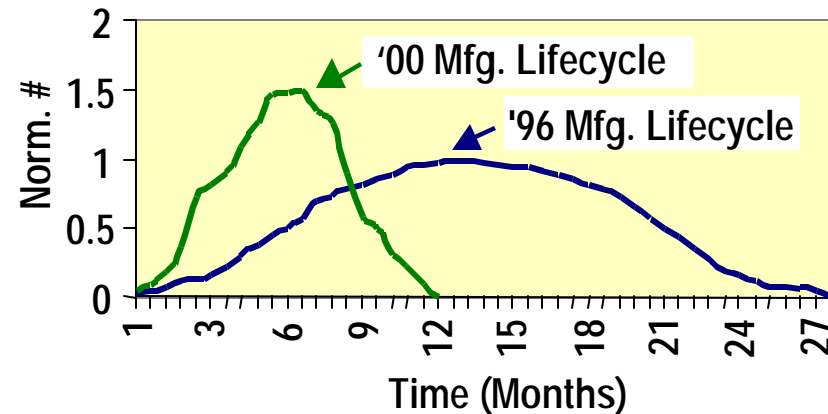
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SOC design opportunities & challenges

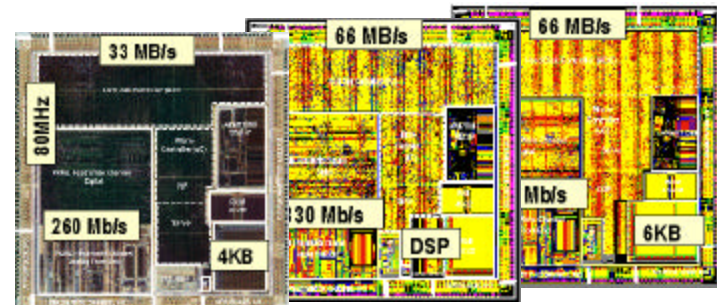
■ First-to-Market & Volume SOCs → Business Success

- ◆ No market ... for a 2nd to market
- ◆ 3-months late = \$500M loss



■ Limited design capacity

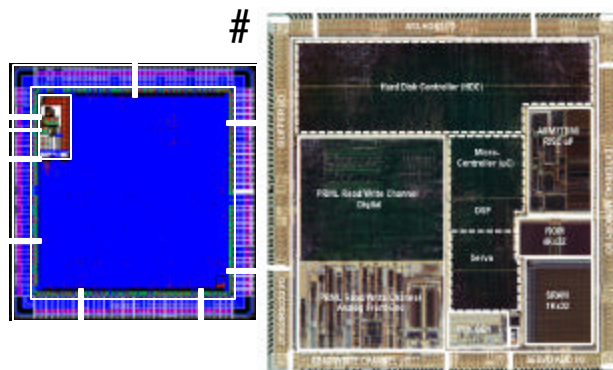
- ◆ Competitive new products roadmap
- ◆ Customize products
- ◆ Access new processes first
- ◆ Multiple sourcing



■ Rapid increase in design complexity

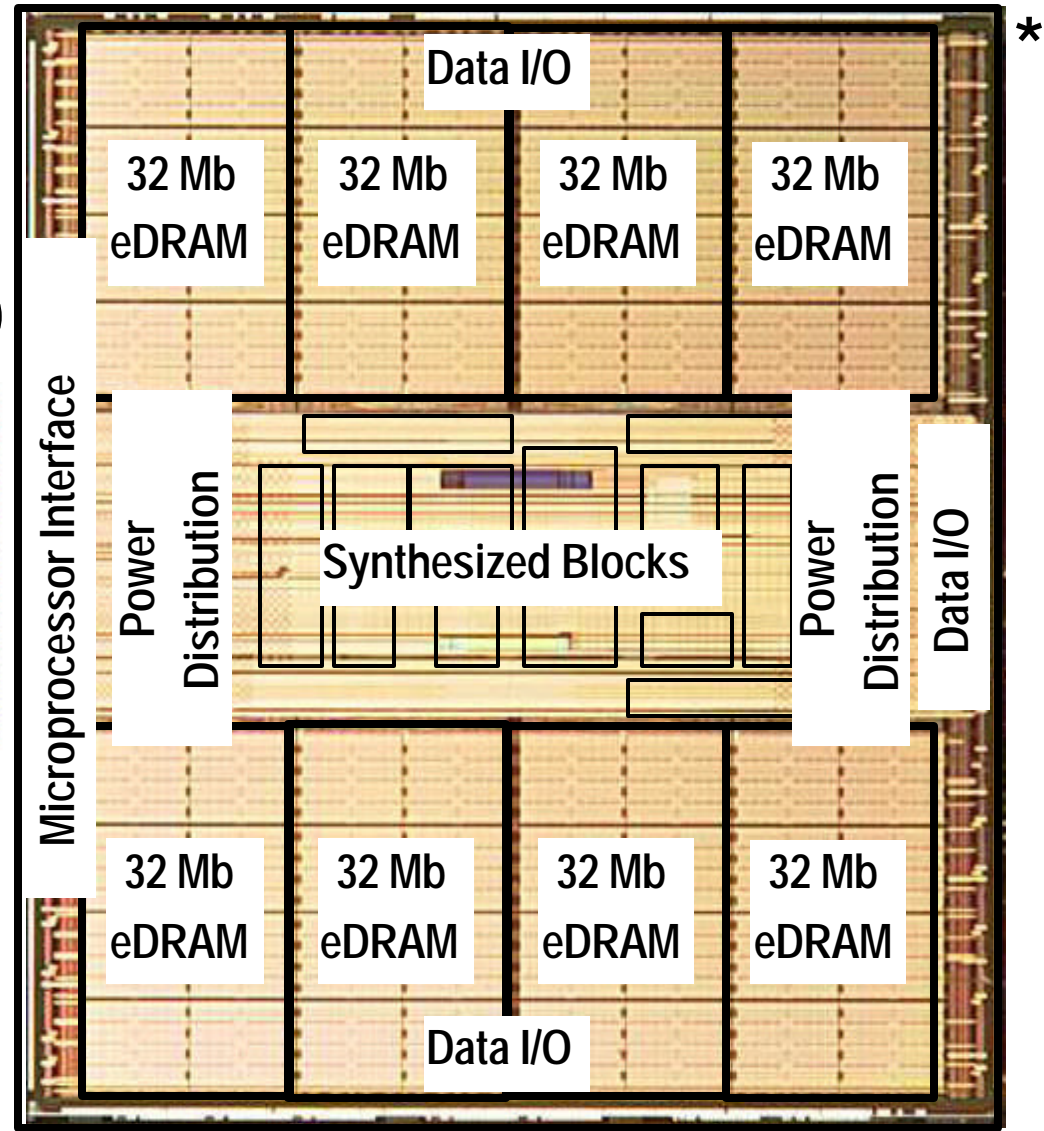
VLSI → SOC: Rapid increase in design complexity

- 0.5um → 0.18um
- 5x5 mm² → 21.7x21.3 mm²
- ~0.8 → 287.5M transistors
- 3LM → 6LM
- ~50 → 150 MHz (#>500MHz)



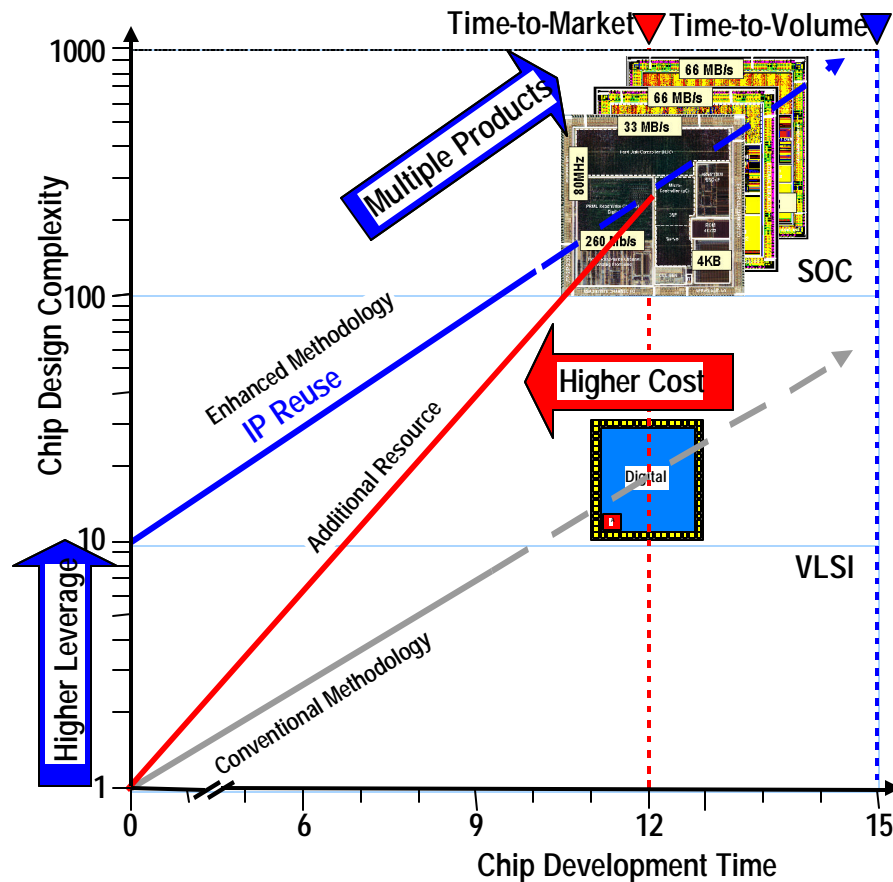
#: Cirrus Logic, Inc. IC, 3Ci™

*: Sony Computer Entertainment, Inc. & Sony Corporation Graphics Synthesizer®I-32. Copyright 2000 Sony Computer Entertainment, Inc. ISSCC2001, 9.6



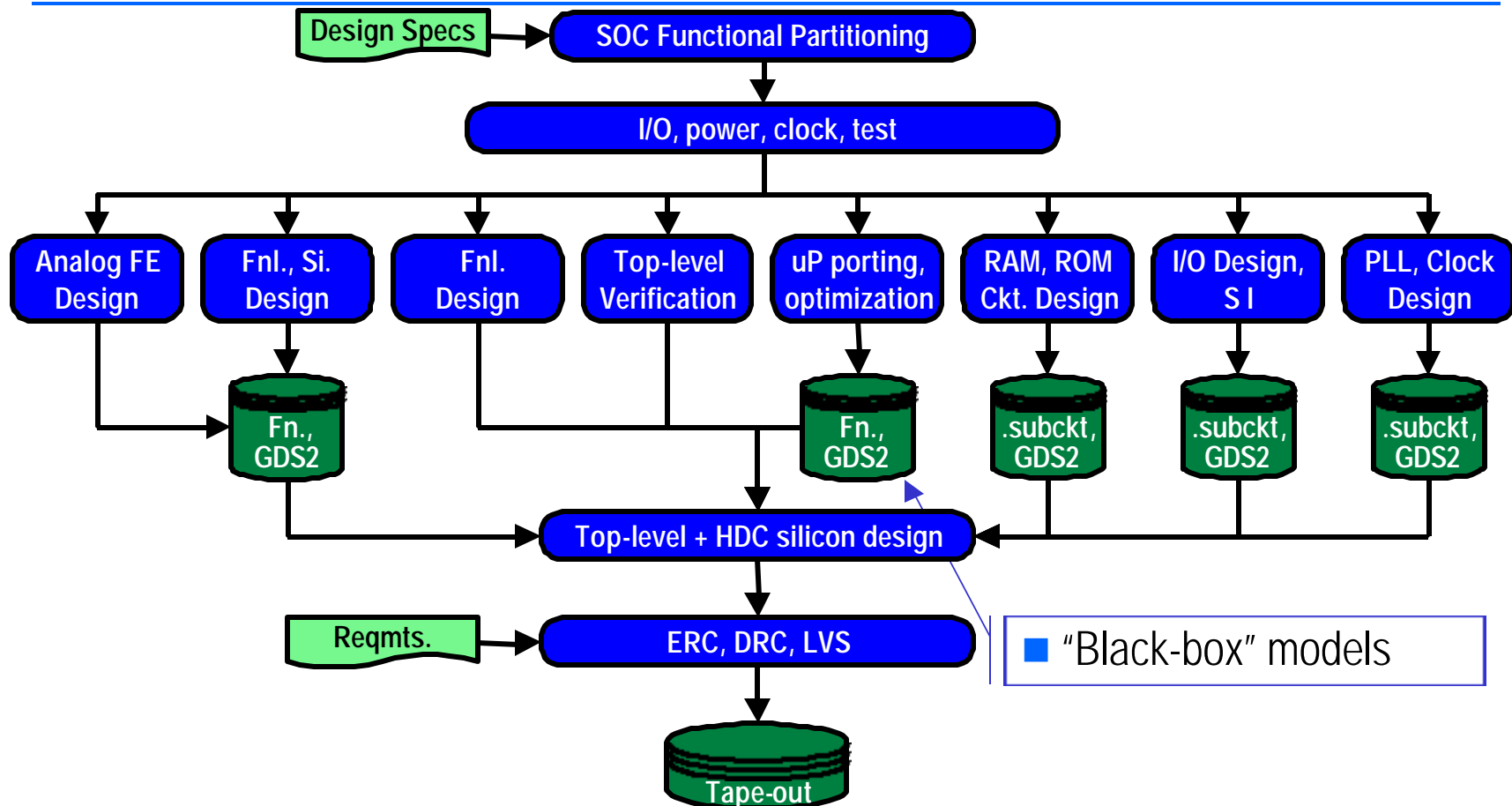
VLSI → SOC: Hierarchical design approach

- SOC Design = IP block creation + block integration



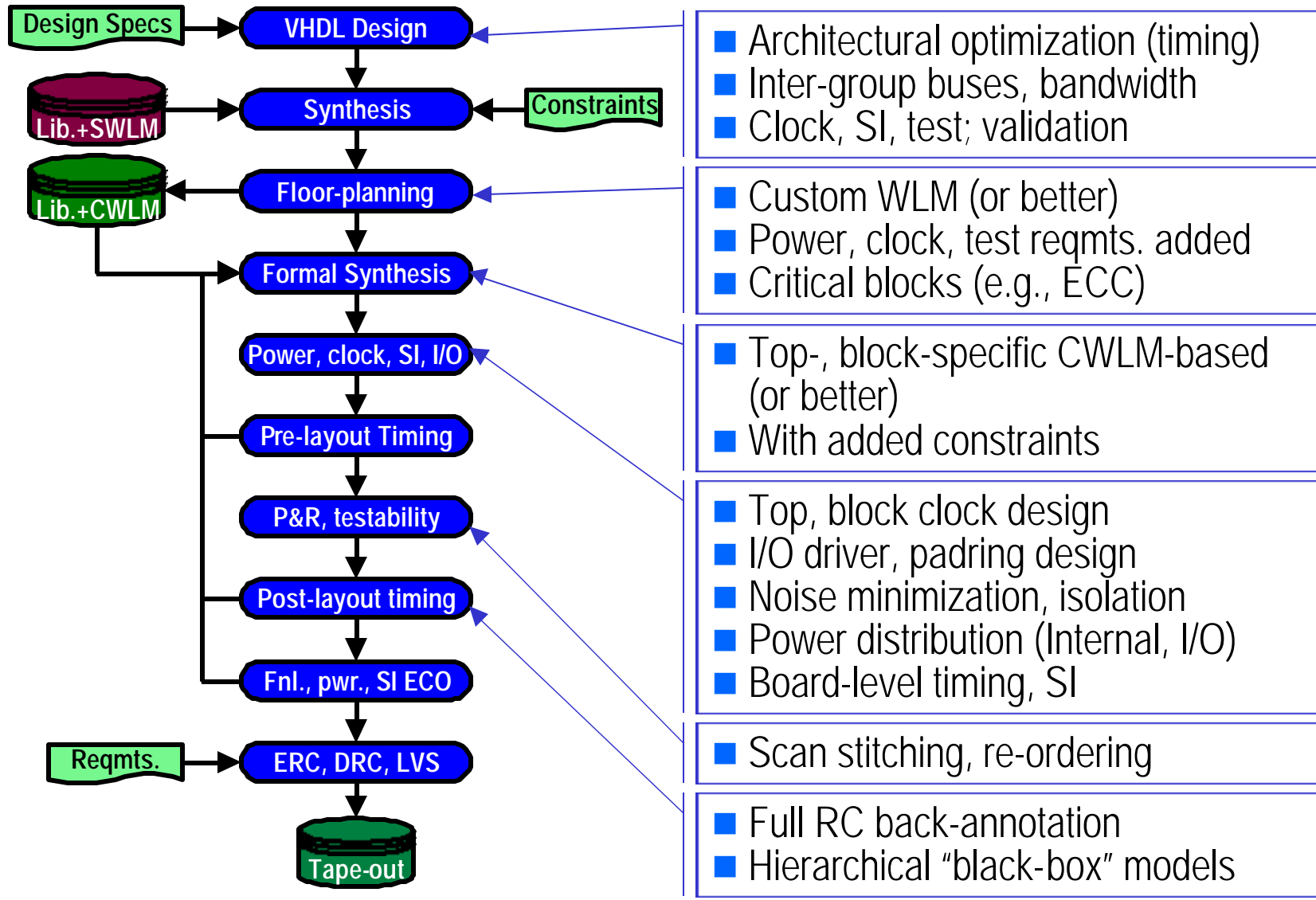
- Enable concurrent engineering
- Reduce development complexity
- Simplify program management
- Leverage proven IP blocks
 - ◆ Improve TTM, TTV and quality
 - ◆ Reduce technical, schedule risks
- Leverage platform infrastructure
 - ◆ Verification, Validation

Top-level SOC design methodology



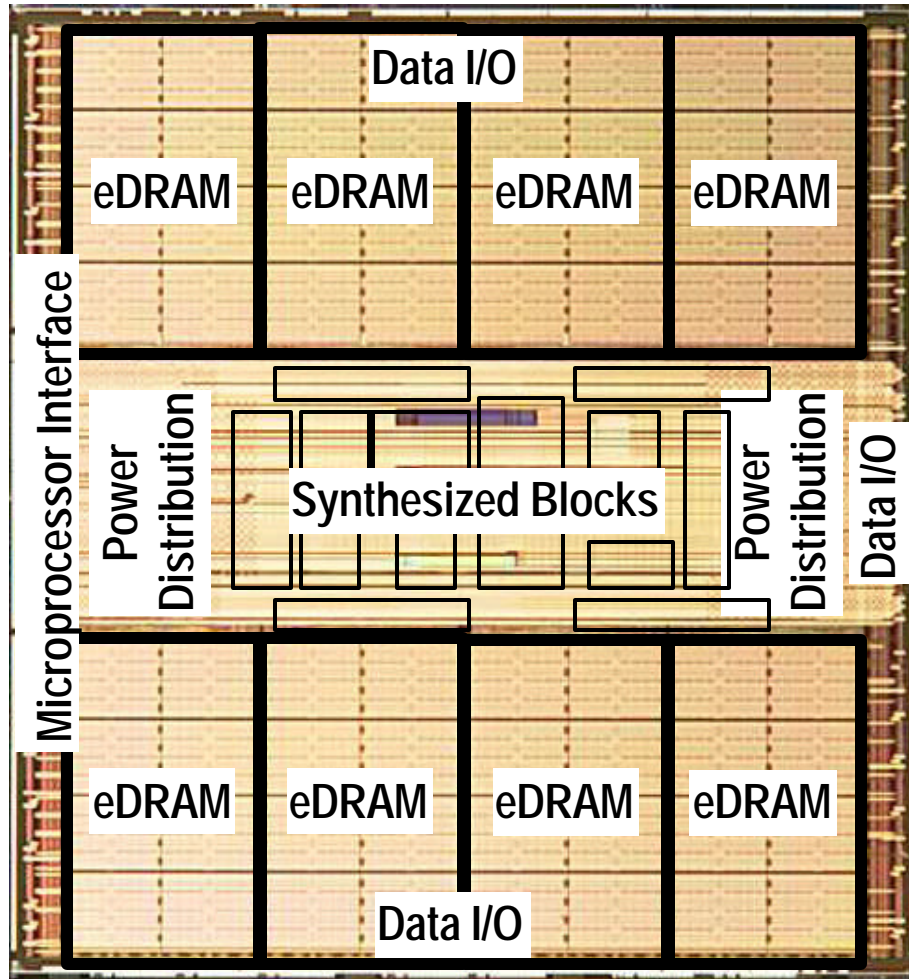
- Functional design → hierarchical
- Electrical / physical design → hierarchical
- IP leverage; Customer-specific design

Block-level design methodology



Sony Computer Entertainment: GS[®]I-32

- Enhanced architecture: 8x higher eDRAM vs. PS[®]2 GS[®]



ISSCC2001 9.6

- Performance

- ◆ eDRAM Bandwidth = 48 GB/s
- ◆ Buses >2K bits wide
- ◆ Render 75M polygons/s

- SOC integration

- ◆ 280M + 7.5M transistors
- ◆ 21.7 x 21.3 mm²

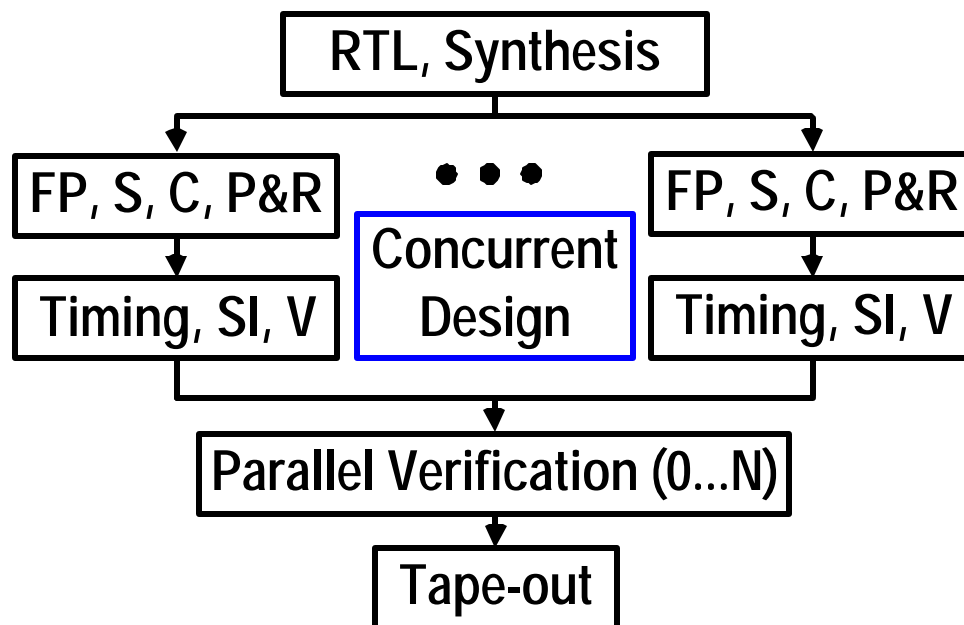
- Scale

- ◆ >400K components
 - 11 blocks, 31K-218K gates
 - >68K flip-flops
- ◆ >500K signal nets
 - >2K nets >10 mm. long

- 0.18 um, 6-metal CMOS

Design approach

- Fully-hierarchical design: Netlist to tape-out in 10 weeks



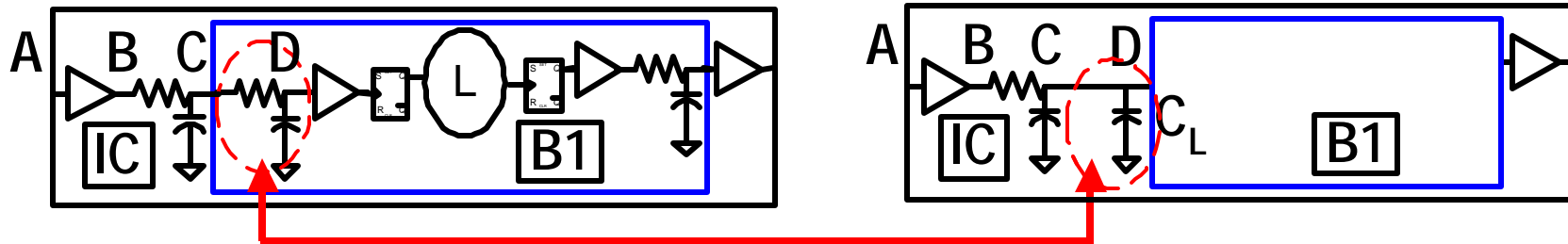
FP: Floorplan
 S: Synthesis
 C: Clock
 P&R: Place-&-Route
 SI: Signal Integrity
 V: ERC, DRC, LVS

- Design challenges

- ◆ Power distribution
- ◆ Clock architecture
- ◆ Timing design
 - Load modeling
 - Delay calculation
- ◆ Signal Integrity
 - Buffer insertion
 - Crosstalk

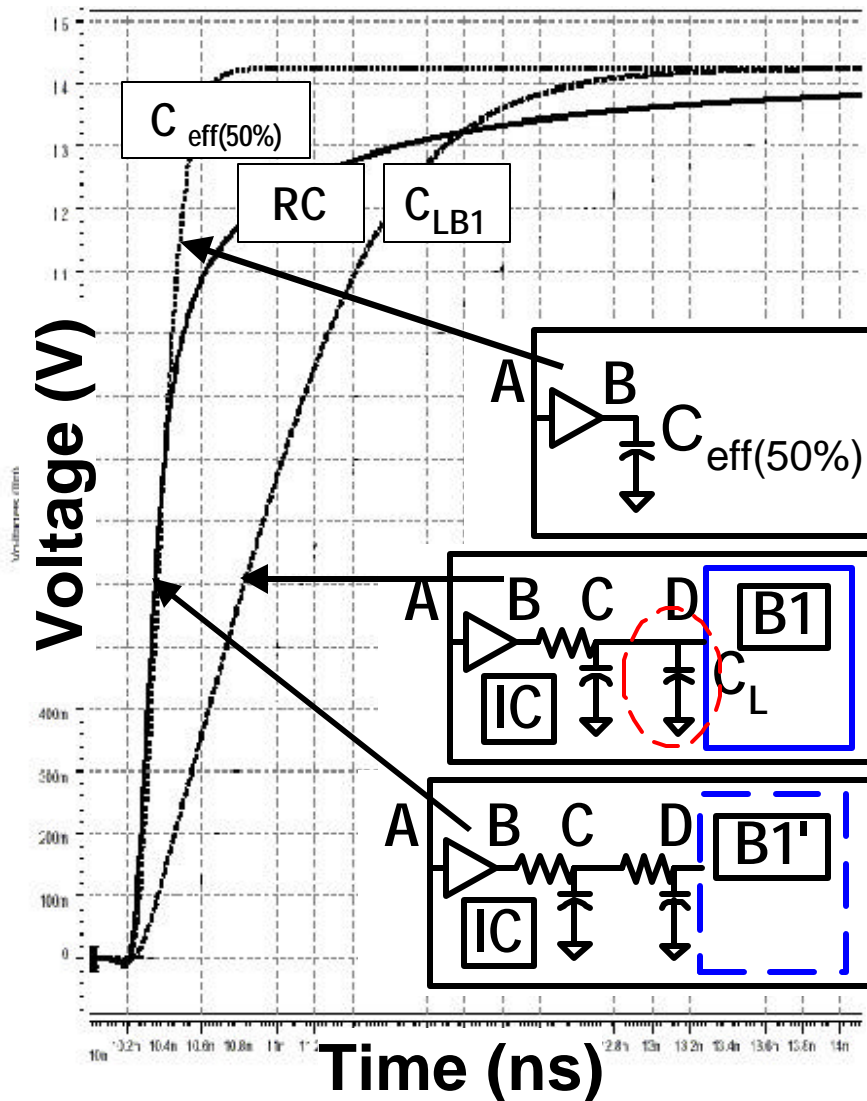
Accurate fully-hierarchical delay calculation

- Fully-hierarchical block-based timing analysis
 - ◆ Analyze large designs (scalable capacity)
 - ◆ Enable concurrent design
 - ◆ Faster timing convergence, verification (STA)
- Signal paths traverse hierarchy
 - ◆ Block inputs with ~0 – 2 mm. metal → RC delay

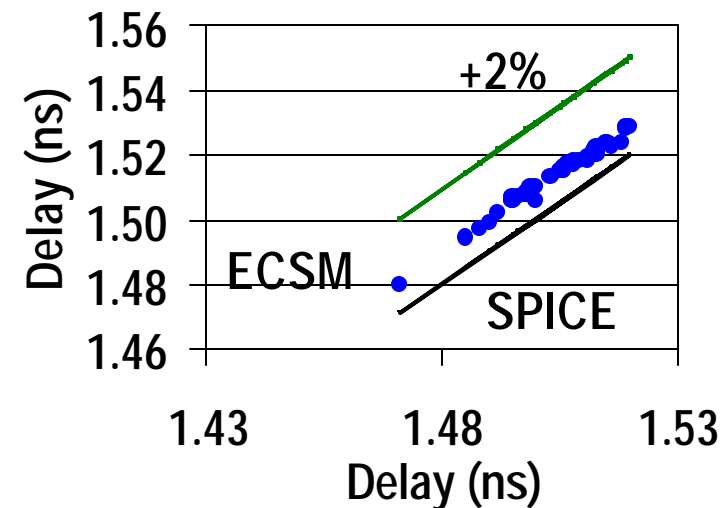


- Model block boundary pin input RC as C_L
- C_L → timing inaccuracies when RC significant

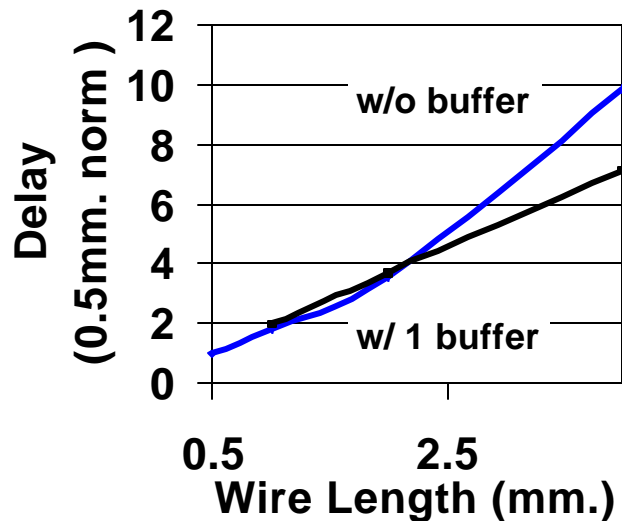
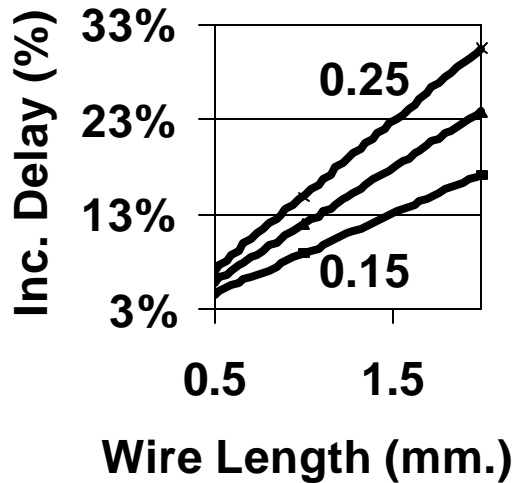
Accurate fully-hierarchical timing



- C_L over-estimates RC delay
 - ◆ Latent hold time defects
 - ◆ Setup \rightarrow overdriven
- ECSM ($C_{eff(50\%)}$) fits SPICE at threshold
- ECSM \rightarrow ~2% correlation to SPICE for complex topologies

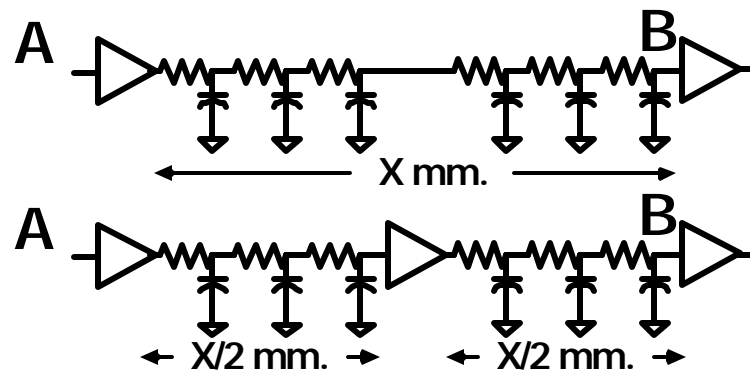


Signal integrity



■ Insert buffers ~1.5 - 2.5 mm.

- ◆ Bound timing uncertainty
- ◆ Reduce total delay



■ Address impact in Static Timing Analysis

- ◆ Reduce setup time margin
- ◆ Bounded hold time margin

IC design → design methodology, technology

- **Hierarchical (mixed-signal) design**
 - ◆ Fully-hierarchical timing: Enhance concurrent design
- **Power distribution**
- **Clocking architecture**
- **New design technology**
 - ◆ Nonlinear delay calculation technology
 - ◆ Black-box, gray-box modeling
 - ◆ Signal integrity
 - RC transmission line effects
 - Crosstalk management
 - Buffer insertion
- **0.15um – 0.13um work**
 - ◆ Technology validation, signal integrity, RLC, substrate, others
- **Focus on silicon engineering: First silicon success**

Related reading

- A. Khan, et. al., "A 150 MHz Graphics Rendering Processor with 256Mb Embedded DRAM," Digest of Technical Papers, pp. 150-151, 442, International Solid State Circuits Conference, February 5-7, 2001, San Francisco
- S. Nassif, "Delay Variability: Sources, Impacts and Trends," pp. 369-69, Digest of Technical Papers, International Solid State Circuits Conference, February 2000
- A. Khan, "Design Challenges in Cirrus Logic, Inc. 3Ci™ System-on-a-Chip Development," SOC Design Seminar, Stanford University, May 1999
- S. Nemazie, A. Khan, et. al., "260 Mb/s Mixed-Signal Single-Chip Integrated System Electronics for Magnetic Hard Disk Drives," Digest of Technical Papers, pp. 42-43, 443, and Slide Supplement 1999 to the Digest of Technical Papers, pp. 44-45, International Solid State Circuits Conference, February 15-17, 1999, San Francisco
- R. Baird, et. al., "A Mixed-Signal 120Msample/s PRML Solution for DVD Systems," Digest of Technical Papers, pp. 38-39, 442, and Slide Supplement 1999 to the Digest of Technical Papers, pp. 40-41, 378 International Solid State Circuits Conference, February 15-17, 1999, San Francisco
- S. Naffziger, "Design Methodologies for Interconnects in GHz+ ICs," International Solid State Circuits Conference Short Course, February 1999
- "Semiconductor Perspectives: Top Ten Stories of 1998," Int'l. Data Corp., 1/99

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